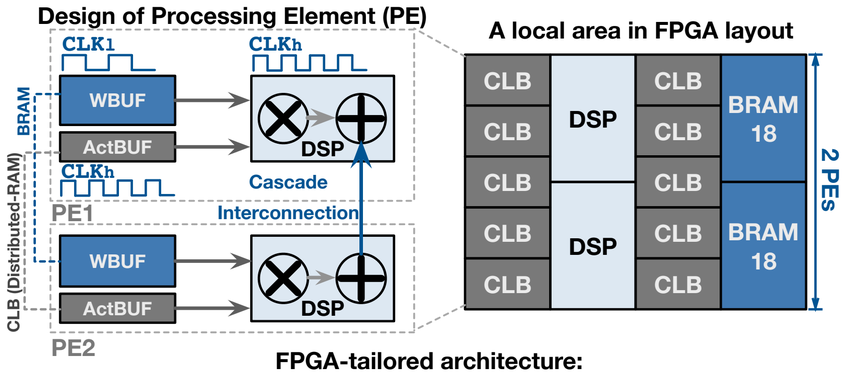
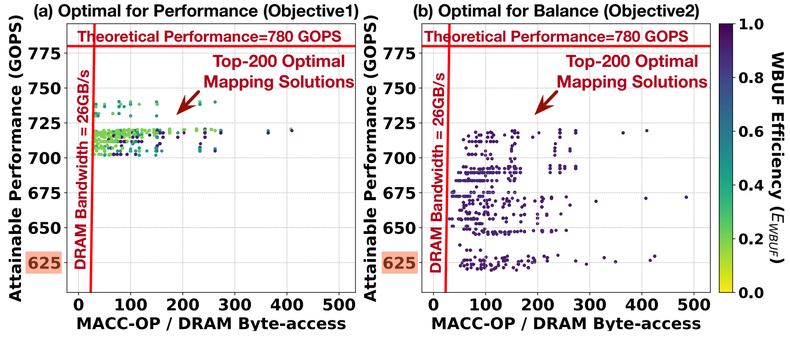
FTDL: An FPGA-tailored Architecture for Deep Learning Systems

- **Problem:** the **architecture-layout mismatch** results in bad timing, anal., drive a Porsche with a bicycle speed.
- **Contribution (HW):** FPGA-tailored design (**good timing**, 650MHz)
- **Contribution (SW):** Compilation (**high hardware efficiency**, 80%+ PE utilization)



FPGA-tailored architecture:
Match the design to FPGA layout, avoiding complex place and routing.

Good Timing
+
High Efficiency
= High Performance



Compilation in FTDL realizes a 80%+ hardware efficiency.